

REMARKS

The application has been carefully review in light of the Office Action dated April 26, 2002. Dependent claim 47 has been amended to correct an error in dependency. A marked-up version of these claims, showing changes made, is attached hereto as Appendix A. Claims 39-48 are still pending in this case. Reconsideration of the above-referenced application in light of the amendments and following remarks is requested.

Claims 39-47 stand rejected under 35 U.S.C. §102(e) as being anticipated by Kawakubo et al. (U.S. Patent No. 5,952,687) ("Kawakubo"). Reconsideration is respectfully requested.

The present application relates to a semiconductor device having an electro-mechanical polished metal layer (claim 39) which may be used as a capacitor electrode (claim 43).

Thus, claim 39 recites a semiconductor device comprising "a substrate, and at least one *electro-mechanical polished* metal layer formed over said substrate" (emphasis added). Similarly, claim 43 recites a semiconductor capacitor comprising "a bottom electrode . . . an insulating layer . . . and a top electrode . . . wherein at least one electrode surface comprises an *electro-mechanical polished surface*" (emphasis added).

Kawakubo discloses a structure with memory cells comprising a charge store element. The charge store element comprises a bottom electrode 13, a high-dielectric layer 14, and a barrier metal film 12 formed in a trench made in the insulating layer 9. Further, portions of the barrier metal film 12, bottom electrode 13, and insulating layer 16 are removed by means of mechanical polishing ("MP") or chemical-mechanical polishing ("CMP") (Figs. 4A-4E, Cols. 7-8). The bottom electrode comprises a noble metal such as platinum. Kawakubo also teaches a polishing stop-layer 10 provided on the flat surface of the insulating layer (Figs. 4A-4E, Col. 5, lines 21-24). Kawakubo does not teach or suggest anywhere that his bottom electrode is an electro-mechanical polished layer.

One skilled in the art knows that MP and CMP techniques, which are taught in Kawakubo, and electro-mechanical polishing (“EMP”) are entirely different processes resulting in significant structural differences. In “Electrochemical Planarization for Multi-Level Metallization of Microcircuitry” by Anthony F. Bernhardt et al. (“article”), disclosed in Applicants’ IDS, CMP is described as possessing “a tendency to *dish down* into the center of wide metal features, as well as causing *scratching and smearing of soft metals*.” (Page 40, Col. 3) (emphasis added). Thus, an EMP processed metal layer will not have the detrimental scratching or smearing associated with a CMP processed metal layer. This is a structural difference.

In contrast to CMP or MP, EMP rotates “the sample during electropolishing [causing] *uniform* electrolyte movement to the entire sample surface, [also] . . . endpoint determination and defect formation” can be monitored in real time (Page 44, Col. 2) (emphasis added). This allows formation of a much smoother surface than comparable processes. Thus, “electrochemical planarization offers *unique advantages* over previous planarization techniques,” including CMP and MP processes (Page 46, Col. 2) (emphasis added). An EMP processed surface has uniformity “within two percent across a 100-mm wafer.” (Page 46, Col. 3). Further still, EMP does not require additives as the CMP process uses (Page 46, Col. 3).

Kawakubo specifically discloses that “where the conductive layer [is] made of soft noble metal such as platinum . . . [and] is subjected to mechanical polishing or chemical-mechanical polishing, the layer *will* undergo so-called metal flow.” (Col. 6, lines 1-2) (emphasis added). To solve this problem, Kawakubo teaches “a noble metal alloy . . . which has a resistivity of 100 [micronOhmscentimeter] or less *and* a Vickers hardness of 80 or more.” (Col. 6, lines 7-10) (emphasis added). In Kawakubo, it is “*necessary* to add an appropriate element to [the] noble metal (e.g., platinum) to provide an alloy which has a sufficient hardness and an adequate electrical conductivity, so that a layer of the alloy may be polished in part to form the bottom electrode.” (Col. 6, lines 24-29) (emphasis). Nowhere does Kawakubo disclose an electro-mechanical polished metal layer.

In fact, Kawakubo teaches adding an additive element such as “a solid-solution

element . . . [or] a precipitation-type element” to the metal that is utilized (Col. 6, lines 30-33). The additive increases the structural hardness and resistivity of Kawakubo’s metal layer so that the metal layer can withstand CMP and MP processing (See Col. 6, lines 33-42). Therefore, Kawakubo’s metal layer differs physically and chemically from Applicants’ claimed EMP polished metal layer.

As is well-known in the art, CMP and MP processes require a downforce of at least two to three pounds per square inch (“psi”). Kawakubo teaches adding an additive element to the metal layer used, thereby increasing the structural hardness of the metal to combat the harmful structural effects of a CMP or MP process. If anything, Kawakubo teaches away from utilizing an EMP polished metal surface. EMP only requires typically, a downforce of around .1 psi. As a result, the surface of an EMP polished metal layer is structurally different from a CMP or MP processed metal surface. An EMP polished metal layer is structurally smoother since the downforce applied does not cause smearing or scratching as a CMP or MP process structurally causes.

Accordingly, Kawakubo does not teach a semiconductor device comprising “a substrate, and at least one *electro-mechanical polished* metal layer formed over said substrate” (emphasis added), as recited in claim 39, or a semiconductor capacitor comprising “a bottom electrode . . . an insulating layer . . . and a top electrode . . . wherein at least one electrode surface comprises an *electro-mechanical polished surface*” (emphasis added), as recited in claim 43. Applicants’ claimed EMP polished metal layer does not require the addition of an additive to combat the harmful structural effects of a CMP or MP process as Kawakubo’s metal layer requires.

The Office Action contends that “it is unclear or not understood how a different surface layer at the metallic surface is achieved or avoided since the material *is the same*.” (Office Action, page 4). Applicants respectfully submit that the materials are not the same. Kawakubo discloses a metal layer combined with an additive. As illustrated in the article, the surface of a CMP or MP processed metal layer will possess scratches and pits as a result of the downforce. However, an EMP polished metal layer, will not possess the scratches and pits that are present in CMP or MP processed metal layer. As discussed above, an

EMP polished metal layer has a significantly superior smoother surface. Kawakubo does not disclose an EMP polished metal layer. This is a significant structural difference at the surface between the claimed invention and cited reference. Note that claim 47, as amended, recites that the bottom electrode consists of platinum, thereby structurally distinguishing over a metal electrode with an additive as in Kawakubo.

Further, applicants' invention can use metal layer's with a Vickers hardness less than 80; whereas Kawakubo's device cannot. This is an additional structural difference.

Kawakubo also teaches a polishing stop-layer. Applicants' invention does not employ a polishing stop-layer. This is an additional structural difference between the present invention and cited reference.

For at least these reasons, independent claims 39 and 43, and dependent claims 40-42 which incorporate all of the limitations of claim 39, and dependent claims 44-47 which incorporate all of the limitations of claim 43, are neither anticipated by, or rendered obvious over Kawakubo.

Claim 48 stands rejected under 35 U.S.C. §103(a) as being unpatentable over Kawakubo et al. (U.S. Patent No. 5,952,687) ("Kawakubo") in view of Sandhu et al (U.S. Patent No. 6,303,956 ("Sandhu")). Reconsideration is respectfully requested.

Claim 48 recites a processor system comprising "a processor . . . a memory device . . . comprising . . . a substrate, and a capacitor . . . comprising at least one electro-mechanically polished layer."

The arguments provided above regarding the rejection of claims 39-47 are equally applicable here. Specifically, electro-mechanically polished metal layers are structurally distinct from layers polished by CMP or MP processes taught in Kawakubo. Sandhu is relied upon as disclosing a memory device electrically coupled to a processor and adds nothing of significance to the issue of electro-mechanically polished layers.

Even if the references could be combined as the Office Action asserts, the

combination of the cited references would not suggest a “a processor . . . a memory device . . . comprising . . . a substrate, and a capacitor . . . comprising at least one *electro-mechanically polished layer*,” as recited by claim 48 (emphasis added). As discussed previously, an electro-mechanically polished layer is structurally different from a CMP or MP polished layer.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to withdraw the outstanding rejection of the claims and to pass this application to issue.

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Respectfully submitted,

By 

Stephen A. Soffen

Registration No.: 31,063

DICKSTEIN SHAPIRO MORIN &
OSHINSKY LLP

2101 L Street NW

Washington, DC 20037-1526

(202) 785-9700

Attorney for Applicants

APPENDIX A

47. (Amended) The capacitor of claim [38] ~~43~~, wherein the bottom electrode [comprises
a] consists of platinum [electrode].